



TULSIRAMJI GAIKWAD-PATIL COLLEGE OF ENGINEERING & TECHNOLOGY

Wardha Road, Nagpur - 441108
Accredited with NAAC A+ Grade & NBA Accredited (EE, ME, CE & ECE)
Approved by AICTE, New Delhi, Govt. of Maharashtra

(An Autonomous Institution Affiliated to Rashtrasant Tukadoji Maharaj Nagpur University, Nagpur)



Department of Electronics and Communication Engineering

Program: B. Tech Electronics and Communication Engineering

Semester-VI | BEC33612: VLSI Design Flow: RTL to GDS-Honour

Teaching Scheme		Examination Scheme (Th)		Examination Scheme (P)	
Theory (Th)	3 Hrs./week	CT-I	15 Marks	-	-
Practical (P)	-	CT-II	15 Marks	-	-
Total Credits	3 (Th) = 3	CA	10 Marks	-	-
Duration of ESE: 3 Hrs.		ESE	60 Marks	-	-
		Total Marks	100 Marks	-	-

Pre-Requisites:

Course Objectives:

1	To understand the fundamentals of VLSI design flow.
2	To learn RTL design using Verilog HDL.
3	To understand logic synthesis and timing analysis.
4	To learn physical design steps, including placement and routing.
5	To understand physical verification and GDSII generation.

Course Content

Unit I	RTL Design: Introduction to VLSI design flow, Verilog HDL basics, Combinational and sequential circuits, RTL coding and simulation, Functional verification
Unit II	Logic Synthesis: Introduction to logic synthesis, RTL elaboration, Technology mapping, Timing, power, and area analysis, Design constraints (SDC), Static Timing Analysis (STA)
Unit III	Floor planning and Placement: Floor planning and chip planning, Core and die sizing, Power planning, Standard-cell placement, Congestion analysis
Unit IV	Clock Tree Synthesis and Routing: Clock Tree Synthesis (CTS), Clock skew and latency, Global and detailed routing, Parasitic extraction, Timing optimization
Unit V	Physical Verification and GDS: Setup and hold timing analysis, Design Rule Check (DRC), Layout Versus Schematic (LVS), Power and signal integrity analysis, Design sign-off GDSII generation and tape-out

Text Books

T.1	M. Morris Mano and Michael D. Ciletti, "Digital Design", Pearson Education, 2017.
T.2	A. K. Singh, "VLSI Design", New Age International, 2011.
T.3	Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", McGraw-Hill Education, 2014.

Reference Books

R.1	Sneh Saurabh, "Introduction to VLSI Design Flow", Cambridge University Press, 2023.
R.2	Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, 2003.
R.3	J. Bhasker and Rakesh Chadha, "Static Timing Analysis for Nanometer Designs: A Practical Approach", Springer, 2009.

Useful Links

1	https://nptel.ac.in/courses/108106191
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CO	Course Outcomes	CL	Class Sessions
CO1	Understand the fundamentals of VLSI design flow.	2	9
CO2	Implement RTL designs using Verilog HDL.	3	9
CO3	Perform logic synthesis and timing analysis.	4	9
CO4	Describe floor planning, placement, clock tree synthesis, and routing.	2	9
CO5	Apply physical verification techniques and understand GDSII generation.	3	9



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